

Self-oscillating Half-bridge Driver

Features

- Floating channel designed for bootstrap operation to +600V
- Noise immunity of transient voltage
- Under-voltage lockout
- Programmable oscillator frequency
- Matched propagation delay for both channels
- Ultra low startup current of 75uA
- Shutdown function turns off both channels
- Low side output in phase with R_T

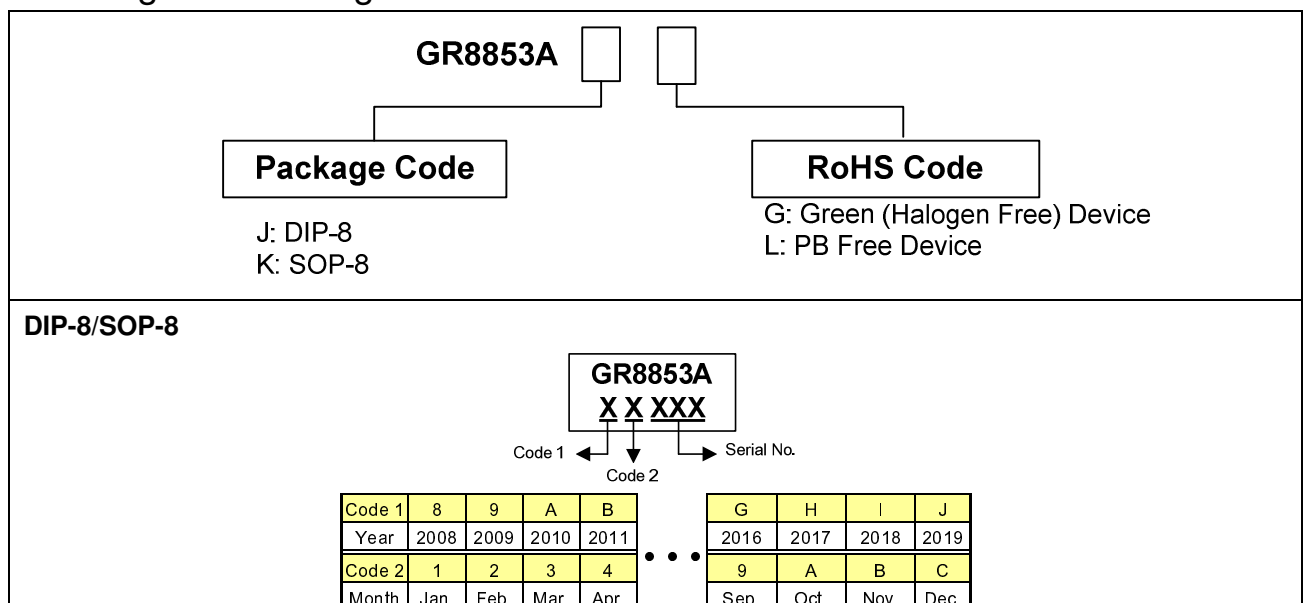
Applications

- HID lamp ballast
- PDP sustain driver
- Motor driver
- SMPS

Description

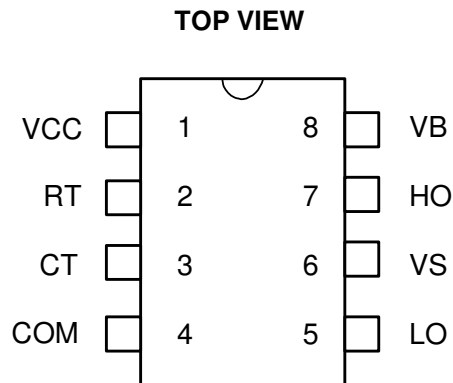
GR8853A is a high voltage, high speed, self-oscillating power MOSFET and IGBT driver with both high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The front end features a programmable oscillator which is similar to the 555 timer. The output drivers feature a high pulse current buffer stage and an internal dead time designed for minimum driver cross-conduction. Propagation delays for the two channels are matched to simplify use in 50% duty cycle applications. The floating channel can be used to drive an N-MOSFET or IGBT in the high side configuration that operates off a high voltage rail up to 600 volts.

Ordering and Marking Information



Greenergy OPTO Inc. reserves the right to make changes to improve reliability or manufacture ability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

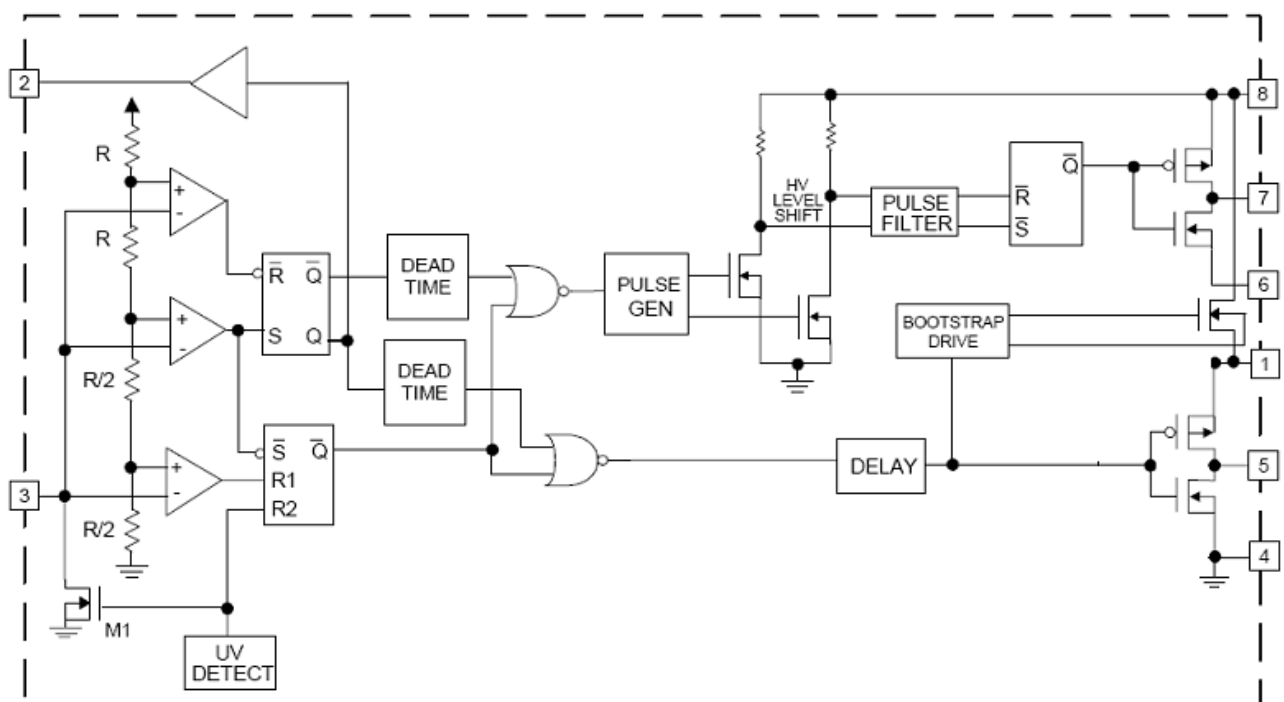
Pin Configuration



Pin Description

Pin No.	Name	Function
1	VCC	Low side and logic fixed supply
2	RT	Oscillator timing resistor input, in phase with HO for normal IC operation
3	CT	Oscillator timing capacitor input, the oscillator frequency according to the following equation: $f = 0.7213 / (RT \times CT)$
4	COM	Low side return
5	LO	Low side gate drive output
6	VS	High side floating supply return
7	HO	High side gate drive output
8	VB	High side floating supply

Block Diagram



Absolute Maximum Ratings

Supply voltage VCC	-----	19V
VB	-----	-0.3V ~ 625V
VS	-----	VB-25V ~ VB+0.3V
HO	-----	VS-0.3V ~ VB+0.3V
LO, RT, CT	-----	-0.3V ~ VCC+0.3V
Junction temperature	-----	150°C
Operating ambient temperature	-----	-20°C ~ 85°C
Storage temperature range	-----	-65°C ~ 150°C
SOP-8 package thermal resistance	-----	160°C/W
DIP-8 package thermal resistance	-----	100°C/W
Power dissipation (SOP-8, at ambient temperature = 85°C)	-----	400mW
Power dissipation (DIP-8, at ambient temperature = 85°C)	-----	650mW
Lead temperature (All Pb free packages, soldering, 10sec)	-----	260°C
ESD voltage protection, human body model	-----	3KV
ESD voltage protection, machine model	-----	200V

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply voltage VCC	10	18	V
Supply voltage VBS	VCC-0.7	18	V

Electrical Characteristics

VBIAS (VCC, VBS) = 12V, CL = 1000 pF, CT = 1 nF and TA = 25°C unless otherwise specified. The VIN, VTH and IIN parameters are referenced to COM. The VO and IO parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
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Low Voltage Supply Characteristics

Rising VCC under-voltage lockout threshold		V_{CCUV+}	8.1	9.0	9.9	V
Falling VCC under-voltage lockout threshold		V_{CCUV-}	7.2	8.0	8.8	V
VCC under-voltage lockout Hysteresis		V_{CCUVH}	0.5	1.0	1.5	V
Micropower startup VCC supply current	$V_{CC} \leq V_{CCUV}$	I_{QCCUV}	—	50	100	μ A
Quiescent VCC supply current		I_{QCC}	—	160	300	μ A
VCC operating voltage		V_{op}	10	12	18	V

Floating Supply Characteristics

Micropower startup VBS supply current	$V_{CC} \leq V_{CCUV}$	I_{QBSUV}	—	0	10	μ A
Quiescent VBS supply current		I_{QBS}	—	30	50	μ A
Offset supply leakage current	$V_B = V_S = 600V$	I_{LK}	—	—	50	μ A

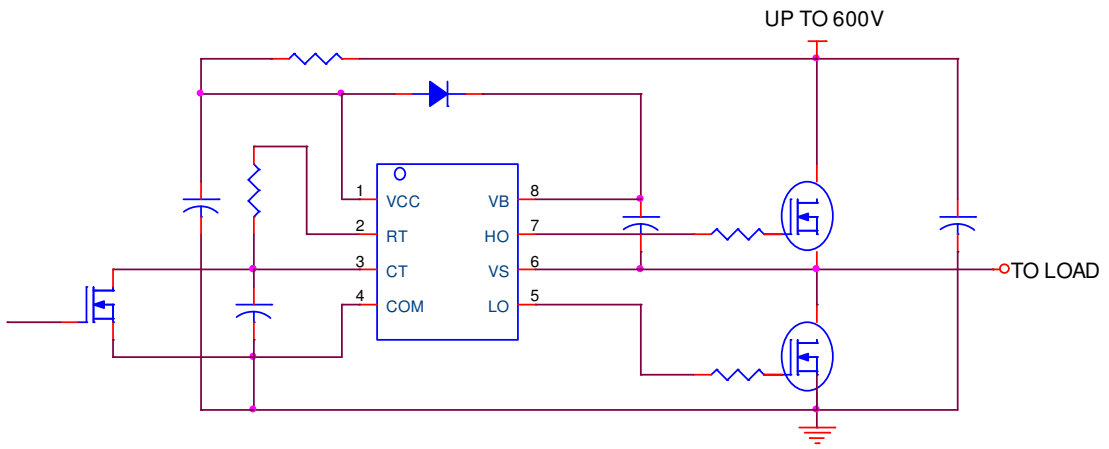
Oscillator I/O Characteristics

Oscillator frequency (CT=1008pF)	$R_T = 14.71k$	f_{osc}	47.2	48.2	49.2	kHz
RT pin duty cycle	$f_{osc} < 100kHz$	d	48	50	52	%
CT pin current		I_{CT}	—	0.001	1.0	μ A
UV-mode CT pin pulldown current	$V_{CC} = 7V$	I_{CTUV}	0.25	0.30	0.5	mA
Upper CT ramp voltage threshold		V_{CT+}	—	8.0	—	V
Lower CT ramp voltage threshold		V_{CT-}	—	4.0	—	V
CT voltage shutdown threshold		V_{CTSD}	3.8	4.1	4.2	V
High-level RT output voltage, VCC - VRT	$I_{RT} = 100\mu A$	V_{RT+}	—	10	50	mV
	$I_{RT} = 1mA$		—	100	300	mV
Low-level RT output voltage	$I_{RT} = 100\mu A$	V_{RT-}	—	10	50	mV
	$I_{RT} = 1mA$		—	100	300	mV
UV-mode RT output voltage	$V_{CC} \leq V_{CCUV}$	V_{RTUV}	—	0	100	mV
SD-Mode RT output voltage, VCC - VRT	$I_{RT} = 100\mu A$	V_{RTSD}	—	10	50	mV
	$V_{CT} = 0V$		—	10	50	mV
	$I_{RT} = 1mA$		—	100	300	mV
	$V_{CT} = 0V$		—	100	300	mV

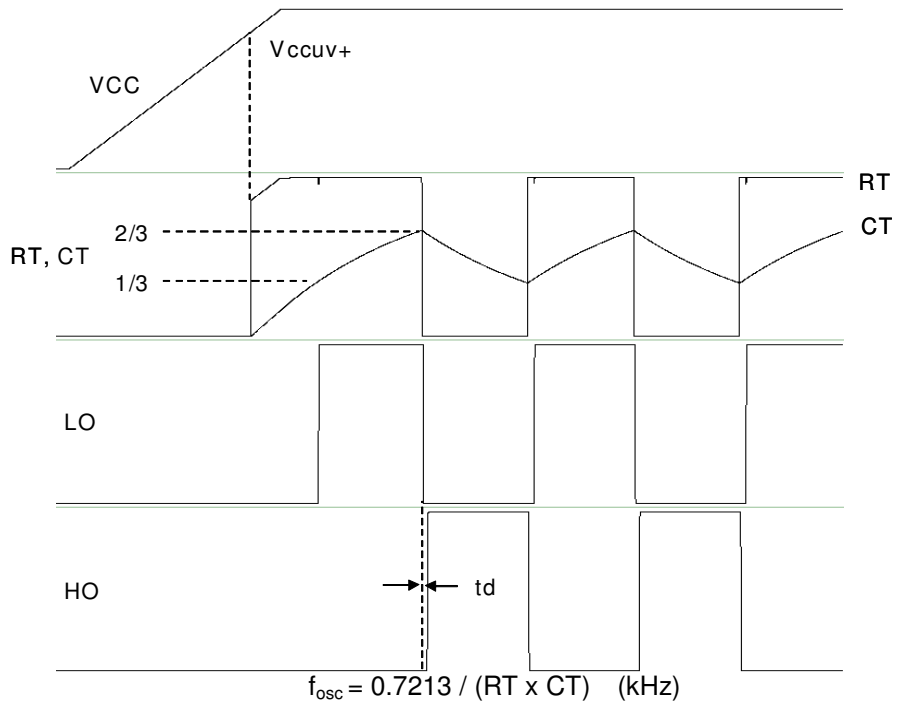
Gate Driver Output Characteristics

Output rise time (CL=1nF)	$V_{CC} \leq V_{CCUV}$	tr	—	80	150	nsec
Output fall time (CL=1nF)		tf	—	30	100	nsec
Shutdown propagation delay		tsd	—	660	—	nsec
Output deadtime (HO or LO)		td	—	1.1	—	μ s

Typical Application Circuit



Input/Output Timing Diagram



Typical Performance Characteristics

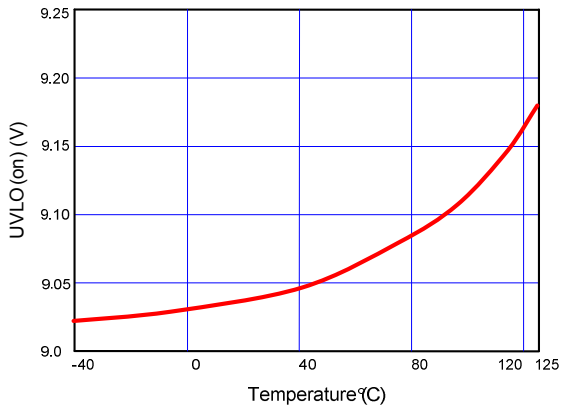


Fig. 1 UVLO(on) vs. Temperature

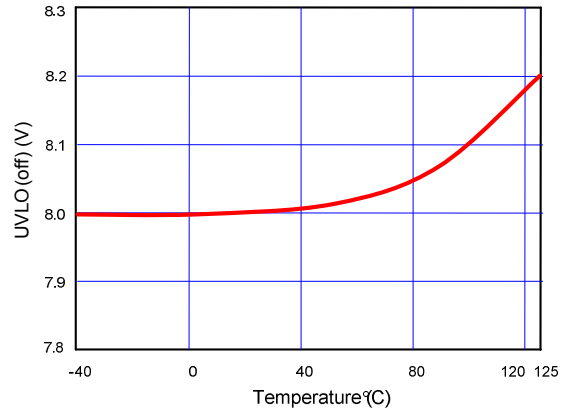


Fig. 2 UVLO(off) vs. Temperature

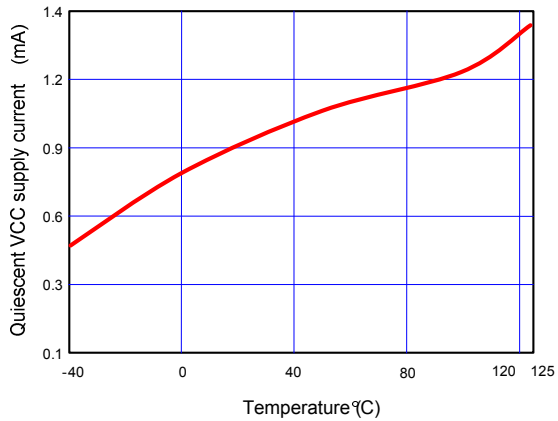


Fig. 3 Quiescent VCC supply current vs. Temperature

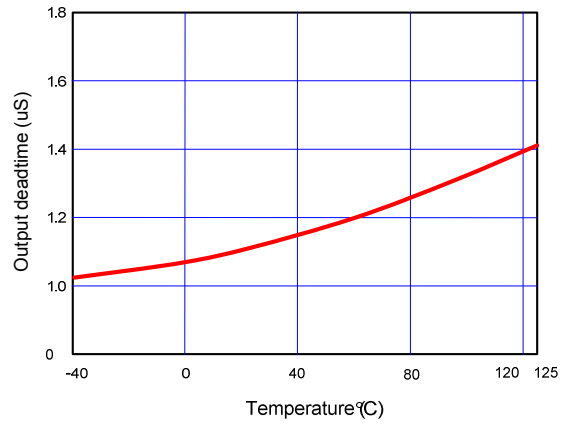


Fig. 4 Output deadtime vs. Temperature

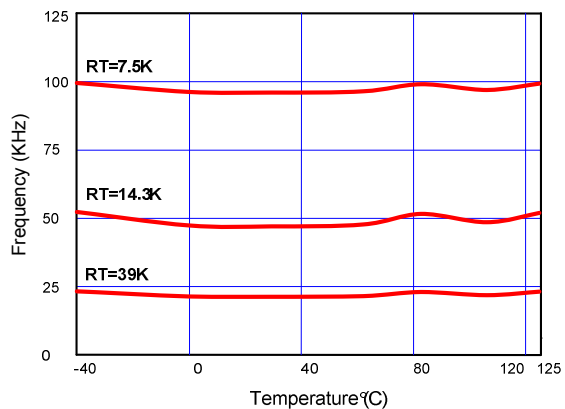
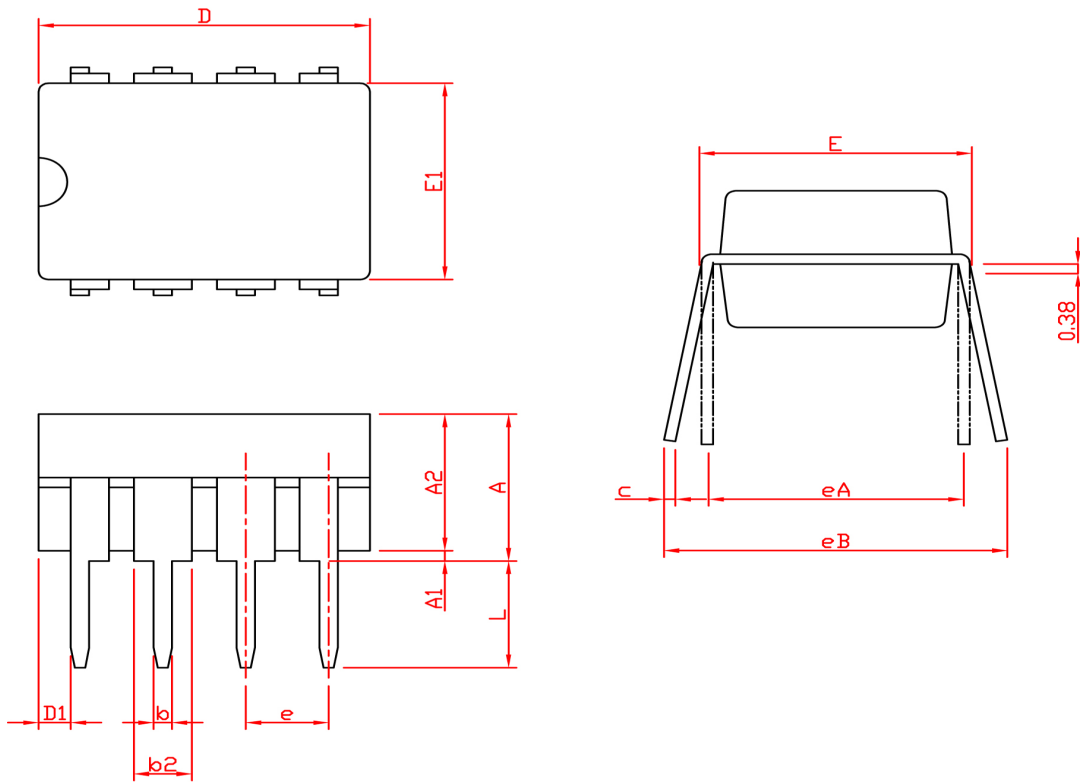


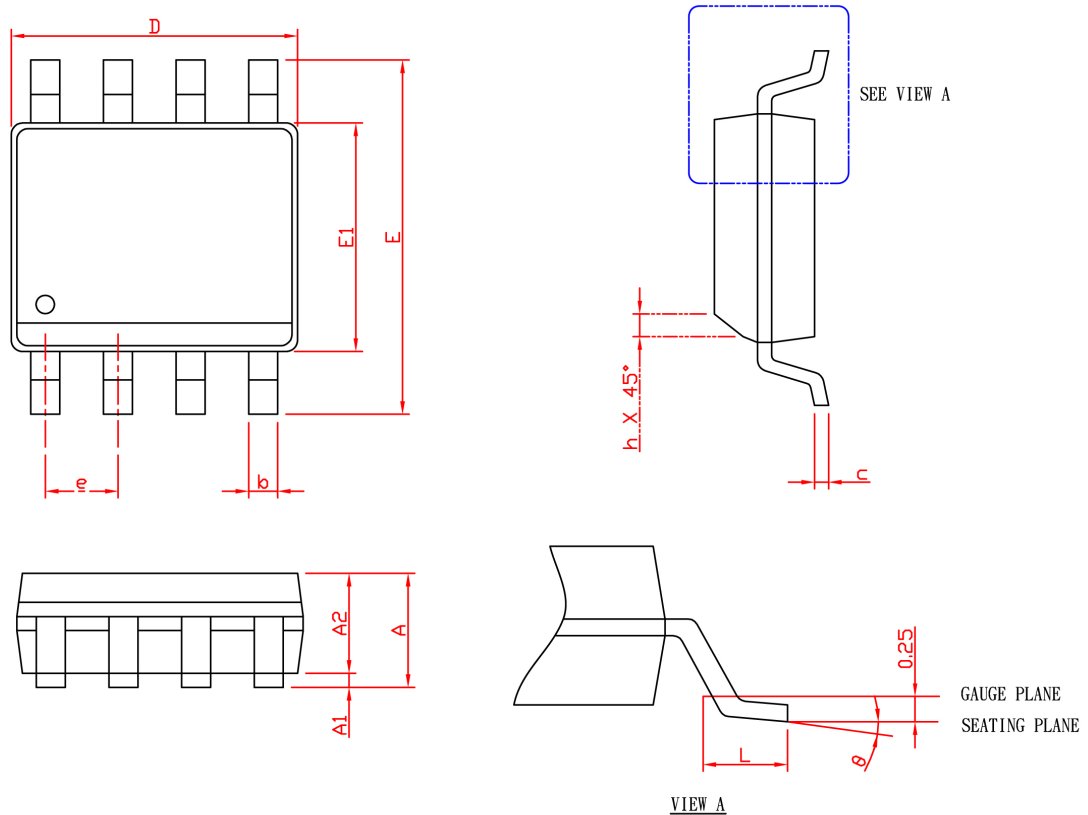
Fig. 5 Frequency vs. Temperature

Package Information


SYMBOL	DIP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	9.01	10.16	0.355	0.400
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
L	2.92	3.81	0.115	0.150

Note: 1. Followed from JEDEC MS-001 BA.

2. Dimension D, D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 10 mil.

Package Information


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

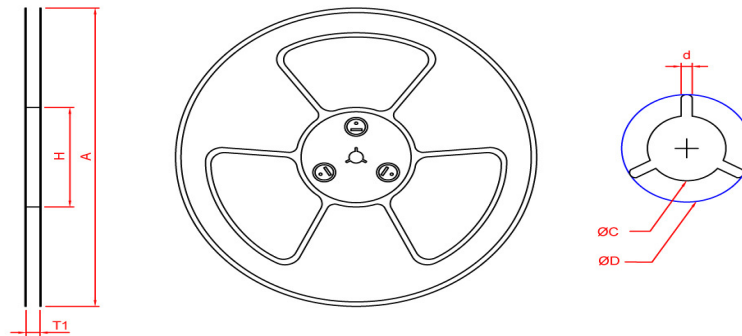
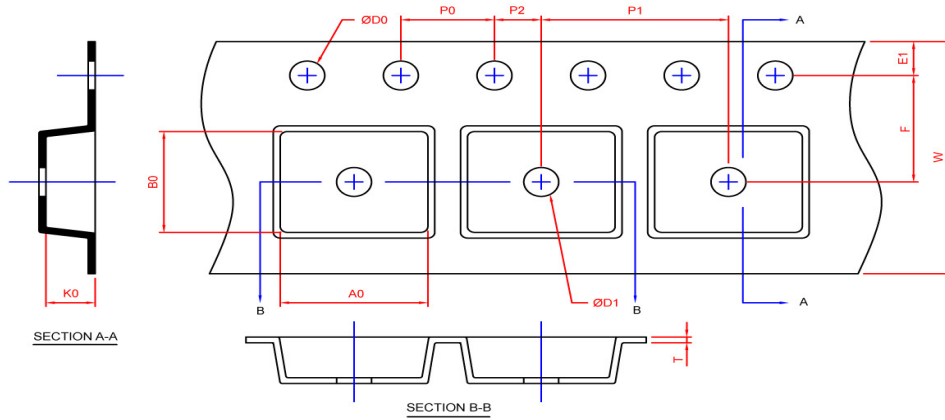
Note: 1. Followed from JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions

SOP-8



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.0	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

Devices Per Unit

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP-8	12	-	2500

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